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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,723	08/25/2003	Ken K. Foo	CS22497RA	2166

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MOTOROLA INC
600 NORTH US HIGHWAY 45
ROOM AS437
LIBERTYVILLE, IL 60048-5343

EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 10/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,723	FOO ET AL.	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,7-9,17, and 19-20* is/are allowed.

6)☒ Claim(s) *1,4,10-12 and 16* is/are rejected.

7)☒ Claim(s) *2,3 and 13-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to Applicant's Amendment dated August 15, 2006 in response to USPTO Office Action dated June 2, 2006.

The cancellation of claims 6 and 18 and the amendments to claims 2, 5, 7-8, 17 and 19 have been considered and entered in the record.

Claim 7 is indicated as being dependent on cancelled claim 6, it is assumed that the intent is to have claim 7 dependent on independent claim 5. Please correct in your next response. For this Action, claim 7 is being considered as being dependent on independent claim 5.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al. (US 2003/0210363) taken with Crossland et al. (USP 5,408,248) in view of Hilbrink (USP 4,641,135).

Relative to claim 1, Yasukawa et al. **teaches** an electrooptical display device (pg. 1, para 0006-0010); Yasukawa et al. further **teaches** a method of activating a display element of a display device having n x m array of display elements, each display element coupled to a logic controlled switch (pg. 7, para. 0090 and Fig. 1).

Yasukawa et al. **does not teach** applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element; applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element; activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Crossland et al. **teaches** addressing crystal cells (col. 1, lines 65-68 and col. 2, lines 1- 47); Crossland further **teaches** applying a row address input and a row electrode input to control logic of the logic controlled switch of the display element; applying a column address input and a column electrode input to the control logic of the logic controlled switch of the display element (col. 4, lines 9-34).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Yasukawa et al. the feature as taught by Crossland et al. in order to put in place the control means to address/refresh specific pixels or groups of pixels.

Yasukawa et al. taken with Crossland et al. **does not teach** activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Hilbrink **teaches** a field effect display system with diode selection of picture elements (col. 2, lines 21-61); Hilbrink further **teaches** activating the display element with the logic controlled switch when the row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Yasukawa et al. taken with Crossland et al. the feature as taught by Hilbrink in order to activate the logic control switch that drives the specific display element designated by the row/column matrix position.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al. taken with Crossland et al. in view of Hilbrink as applied to claim 1 in item 3 hereinabove, and further in view of Togashi (USP 4,345,249) taken with Santoro et al. (US 2003/0020671).

Regading claim 4, Togashi **teaches** a liquid crystal display panel (col. 2, lines 53-68 and col. 3, lines 1-20); Togashi further **teaches** activating a first set of at least some display elements of the display device; and activating a second set of display elements of the display device (col. 2, lines 53-63).

Togashi **does not teach** driving the first set of elements at a first refresh rate and driving the second set of elements at a second refresh rate different than the first refresh rate.

Santoro et al. **teaches** a system for the simultaneous display of multiple information source (pg. 2, para. 0019 and pg. 3, paras. 0020-0024); Santoro et al. further teaches driving the first set of elements at a first refresh rate and driving the second set of elements at a second refresh rate different than the first refresh rate (pg 3, para 0020).

It would have been obvious to a person of ordinary skill in the art at the time of the invention

to provide to the device as taught by Yasukawa et al. taken with Crossland et al. in view of Hilbrink and further in view of Togashi the feature as taught by Santoro et al. in order to put in place the means to refresh different regions or the display screen as different refresh rates in order to preserve power by using lower refresh rate when it is practical to do so.

5. Claims 10-12 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yasukawa et al. taken with Crossland et al. in view of Hilbrink as applied to claim 1 in item 3 hereinabove, and further in view of Martin et al. (USP 6,094,704).

Regading claim 10,Yasukawa et al. taken with Crossland et al. in view of Hilbrink **does not teach** a display device with an addressable latch having a row addressed input and a column address input.

Martin **teaches** a memory device with row and column address paths (col. 4, lines 57-67 and col. 5, lines 1-29); Martin further **teaches** a display device with an addressable latch having a row addressed input and a column address input (col. 9, lines 59-64).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Yasukawa et al. taken with Crossland et al. in view of Hilbrink the feature as taught by Martin in order to put in place the logic element with the means to accept the row address and column address input signals and in turn generate an output signal to activate a particular display element.

Relative to claim 11, Crossland et al. further **teaches** display device with an addressable latch having a row electrode input and a column electrode input (col. 4, lines 9-20).

Regading claim 12, Martin et al. further **teaches** a display device wherein the addressable latch of each display element including row address logic an column address logic having

corresponding outputs coupled to the output of the addressable latch, the row address input coupled to the row address logic, and column address input coupled to the column address logic (col. 9, lines 59-64).

Regarding claim 16, Yasukawa et al. further **teaches** the display is a thin-film transistor display device (pg. 7, para. 0090).

Allowable Subject Matter

6. Claims 2-3 and 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 2, the major difference between the teachings of the prior art of record (Yasukawa et al. (US 2003/0210363), Crossland et al. (USP 5,408,248) and Hilbrink (USP 4,641,135) and that of the instant invention is that said prior art of record **does not teach** the method steps of comparing the row address input and the row electrode input, comparing the column address input and the column electrode input, activating the display element with the logic controlled switch based on results of the comparisons.

Relative to claim 13, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display device wherein the addressable latch of each display element including first and second comparators, the first comparator having the row address input and a row electrode input, the second comparator having the column address input and a column electrode input, each display element including a logic device having a first input coupled to an output of the corresponding first

comparator the logic device having a second input coupled to an input of the corresponding second comparator.

7. Claim 5, 7-9, 17 and 19-20 are allowed.

8. The following is an examiner's statement of reasons for allowance:

Relative to claim 5, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a method in a display device comprising: an n x m array of addressable display elements, the method comprising: activating at least some display elements characterizing a foreground image at a first rate; activating other display elements characterizing a background image at a second rate, the second rate less than the first rate; activating the display elements with a corresponding logic controlled display element switch when row address and row electrode inputs and when the column address and column electrode inputs satisfy a condition.

Relative to claim 17, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a method in a display device comprising an n x m array of addressable display elements, the method comprising: selectively activating display elements by individually addressing the display elements to be activated, activating the display elements includes, applying a row address input and a row electrode input to control logic of the corresponding display element, applying a column address input and a column electrode input to the control logic of the corresponding display element, and activating the display element with a logic controlled switch when the control logic inputs satisfy a condition; reducing power consumption by addressing at least some

of the display elements at a first frequency and addressing other display elements at a second frequency, the second frequency less that the first frequency.

Response to Applicant's Remarks

9. Applicant's Remarks relative to claims 1, 4, 10 and 11 are rendered moot with the introduction of new prior art in the rejection of said claims 1, 4 10 and 11.

Applicant's Remarks regarding claims 5 and 17 are rendered moot in light of the allowance of said claims 5 and 17.

Applicant's remarks regarding claim 2 are rendered moot in light of the change in status of claim 2 from being 'rejected' to 'objected to'

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,476,914	Hoelzi et al.
U. S. Patent No	5,774, 104	Crossland et al.
Pub. No.	UIS 2006/0209009	Schlangen et al.

To Respond

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent E. Kovalick
October 3, 2006

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600